

Abstract of the Disclosure

An integrated circuit die and method of fabricating the same. The method comprises further grinding, polishing or otherwise treating one or more perimeter edges of an individual circuit die. The perimeter edges are treated to remove a substantial
5 portion of the remaining substrate material layer or scribe therefrom without exposing the active circuitry of the die. The process reduces the overall length and width dimensions of a die producing a smaller circuit die without reducing the amount of circuitry on the die.

10

"Express Mail" mailing label number: EL671638662US

Date of Deposit: February 16, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.
